DESCRIPTION

WF4455 is a high performance OOK/ASK transmitter for the Remote Keyless Entry (RKE) systems. It consists of a power amplifier, one-shot circuit and phase-locked loop with internal voltage controlled oscillator and loop filter. The one-shot circuit control the phase-locked loop and power amplifier to have fast start-up time in operation.

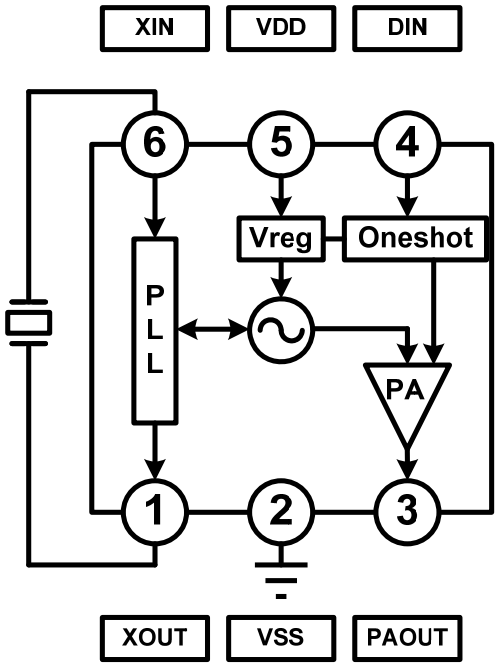
FEATURES

- Highly integrated OOK/ASK transmitter
- High output power, 3 V /+11 dBm / 17 mA
- Low supply voltage, 2.2 V to 3.6 V operation range
- Low external component cost.
- PLL-based transmitter with frequency range from 250MHz to 450MHz
- On-chip one-shot circuit
- 60 dB RF on-off ratio for OOK/ASK modulation
- SOT23-6 package

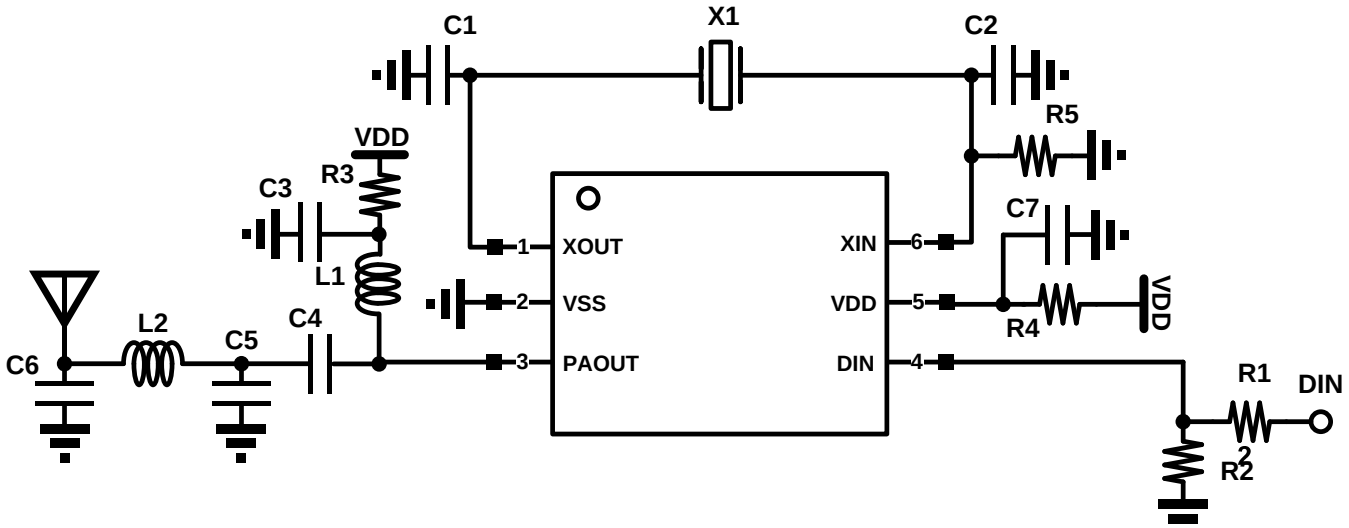
APPLICATIONS

- Keyless entry systems
- Remote control systems
- Garage door openers
- Alarm systems
- Security systems
- Wireless sensors

BLOCK DIAGRAM



APPLICATION CIRCUIT



BILL OF MATERIALS

Part	Value		Unit
	315MHz	433.92MHz	
X1	9.844M	13.56M	Hz
R1	10K	10K	Ω
R2	100K	100K	Ω
R3	0	0	Ω
R4	0	0	Ω
R5	560K	560K	Ω
C1	22p	18p	F
C2	22p	18p	F
C3	1μ	1μ	F
C4	220p	220p	F
C5	8.2p	4.7p	F
C6	18p	10p	F
C7	2.2μ	2.2μ	F
L1	180n	180n	H
L2	33n	27n	H

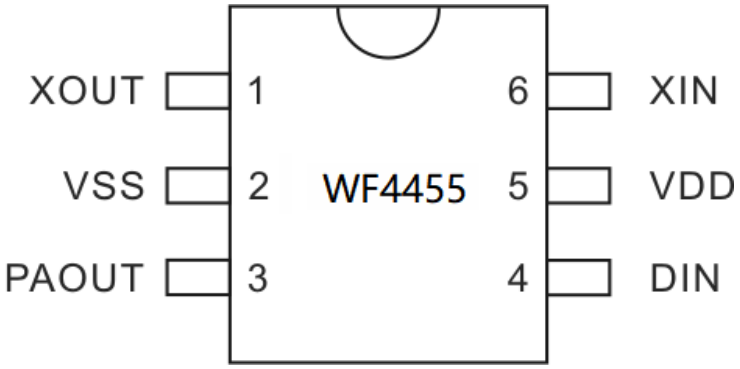
Notes:

1. C1/C2 can be used to trim the transmitted signal frequency for matching the specified value.
2. L2/C5/C6 value will depend on PCB layout.
3. The recommend maximum ESR value of X1 is 40Ω.
4. To populate the R5 over XIN will help to maintain good oscillation in high X1 ESR.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
WF4455	6 Pins, SOT23	WF4455

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
XOUT	O	Oscillator output	1
VSS	G	Ground connection	2
PAOUT	O	Power amplifier output	3
DIN	I	Data input	4
VDD	P	Power supply	5
XIN	I	Oscillator input	6

FUNCTION DESCRIPTION

PA OUTPUT MATCHING

The PA output is an open-drain structure. Its output connects a large choke inductor to supply voltage and follows by a DC block capacitor. After the DC block capacitor, a C-L-C π-type matching network is used to tune with the antenna impedance. The inductor and capacitor values may be different from the suggestion value depending on PCB material, PCB thickness, ground configuration, and the layout traces length.

For the open-drain structure in PA, the HBM (Human Body Mode) and MM (Machine Mode) ESD strength is 4KV and 400V.

REFERENCE OSCILLATOR

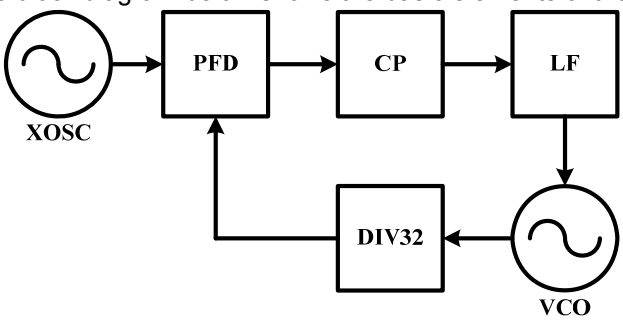
For a quartz crystal to oscillate in the specified frequency, it should work with vendor provided load capacitor value, called C_L. The load capacitor is about 12pF to 18pF in general. In WF4455, the Piercetype crystal oscillator is used, and the shunt capacitor over XIN and XOUT is in series together equivalently. The shunt capacitor should be placed as 2x C_L to oscillate with specified frequency. The temperature coefficient of quartz crystal will cause the VCO output frequency drift in high/low temperature range.

With a fixed divided-by-32 PLL, the f_{REFOSC} = f_{TX} / 32. The following table list f_{REFOSC} for some common transmit frequencies

Transmit Frequency f_{TX}	Reference Oscillator Frequency f_{REFOSC}
315 MHz	9.844 MHz
340 MHz	10.625 MHz
390 MHz	12.188 MHz
433.92 MHz	13.56 MHz

PHASE-LOCKED LOOP (PLL)

The WF4455 own a fixed divided-by-32 PLL to generate the transmitter signal. The PLL consists of the voltage-controlled oscillator (VCO), crystal oscillator, asynchronous ÷32 divider, charge pump, loop filter and phase-frequency detector (PFD). All these circuits are integrated on-chip. The PFD compares two signals and produces an error signal which is proportional to the difference between the input phases. The error signal passes through a loop filter with an approximately 180 KHz bandwidth, and is used to control the VCO. A frequency divider placed after the VCO and it will feedback the divided signal to PFD. In the final the VCO will get locked to reference signal as f_{VCO} = f_{REFOSC} * 32. The block diagram below shows the basic elements of the PLL.



The PLL chain circuit is supplied by internal voltage regulator to ease the PA pulling and crystal spur issue

ONE-SHOT CIRCUIT AND POWER-DOWN CONTROL

During the signal transmission, the crystal oscillator start-up time will limit its wake-up time to work. A one-shoot circuit is used to solve this problem by turning on/off the power amplifier and PLL circuit separately.

When apply “HIGH” to DIN, will enable the PLL chain and PA. When applied “LOW” to DIN, the PA will be turn-off immediately, and the PLL chain will be turn-off after one-shot period about 50ms.

To calculate the re-triggerable one-shot delay time, it can be counted as 688128 / f_{REFOSC} . For f_{REFOSC} = 9.844MHz and 13.56MHz, the delay time is about 70ms and 50ms.

ANTENNA DESIGN AND PCB LAYOUT CONSIDERATION

For a λ/4 dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}$$

For example, if the frequency is 315 MHz, then the length of a λ/4 antenna is 22.6 cm. If the calculated antenna length is too long for the application, then it may be reduced to λ/8, λ/16, etc. without degrading the input return loss. Usually, when designing a λ/4 dipole antenna, it is better to use a single conductive wire (diameter about 0.8 mm to 1.6 mm) rather than a multiple core wire.

If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (ε_r = 4.7) and a strip-width of 30 mil, the length of the antenna, L (in cm), is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where “c” is the speed of light (3 x10^{10} cm/s)

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. Grounding the metal case of quartz crystal and isolate the XIN/XOUT trace to other can suppress the crystal spur signal over PA output.

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD}	-0.3	5	V
I/O Voltage	$V_{I/O}$	-0.3	5	V
Operating Temperature Range	T_A	-40	+85	°C
Storage Temperature Range	T_{STG}	-55	+125	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD}	-0.3	3.6	V
Operating Temperature Range	T_A	-40	+85	°C

ELECTRICAL CHARACTERISTICS

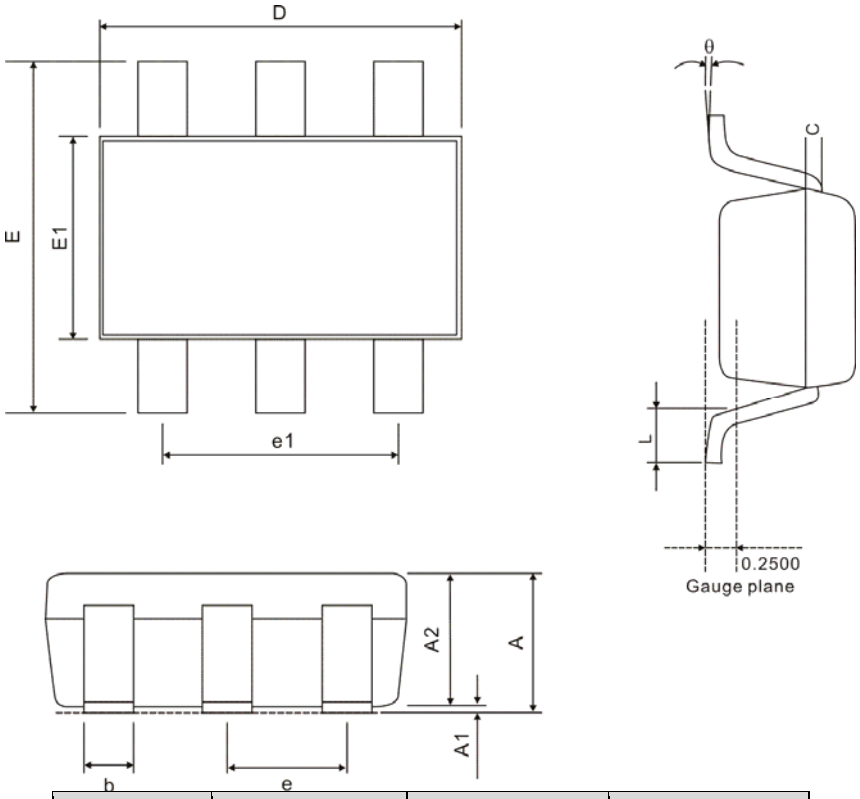
Nominal conditions: V_{DD} = 3.0 V, V_{SS} = 0 V, T_A = +27°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD}		2.2	3.0	3.6	V
Operating Current (Note)	I_{DD}	DIN=High(CW mode); P_{OUT} =12dBm, f_{RF} = 315MHz		17		mA
		DIN=High(CW mode); P_{OUT} =10dBm, f_{RF} = 434MHz		19		mA
Standby Current	$I_{standby}$	DIN=Low; T_{DELAY}>50ms			1	μA
RF						
Frequency Range	f_{RF}		250		450	MHz
Power Amplifier Output Power (Note)	P_{out}	f_{RF} = 315MHz		11		dBm
		f_{RF} = 434MHz		10		dBm
RF Power On / Off Ratio	P_{EXT}			60		dB
Phase Noise	P_{NOISE}	315MHz, 10KHz offset		-75		dBc/Hz
Harmonics (Note)	P_{HARM}	2x/3x f_{RF}		-40		dBc
Crystal Spur	P_{SPUR}	f_{RF} = 315MHz		-50		dBc
		f_{RF} = 434MHz		-50		dBc
Data Input and One-shot						
Data Rate	D_{RATE}		0.5	2	50	Kbps
Crystal Oscillator Start-up Time	T_{ON}	C_L not connected		1		ms
One-shot Delay Time	T_{DELAY}		50			ms

Note: Depend on power amplifier output matching

PACKAGE INFORMATION

6 Pins, SOT23-6



Symbol	Min.	Nom.	Max
A	-	-	1.45
A1	0.00	-	0.15
A2	0.90	1.15	1.30
b	0.30	-	0.50
c	0.080	0.130	0.200
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
e1	1.90 BSC		
θ	0°	-	8°
L	0.30	0.45	0.60

Notes;
1. Refer to JEDEC MO-178
2. All dimensions are in millimeter